CLAIMS

What is claimed is:

1. An electronic circuit for receiving a differential mode signal on a first pair of conductors and transmitting a signal on a second pair of conductors, the circuit comprising:

a first steering circuit responsive to the differential mode signal on the first pair of conductors for generating a signal on one of the second pair of conductors; and

a second steering circuit responsive to the differential mode signal on the first pair of conductors for generating a signal on the other of the second pair of conductors.

2. A circuit in accordance with claim 1, further comprising:

circuitry responsive to application of a DC voltage level disabling the first steering circuit.

3. A circuit in accordance with claim 2, further comprising:

circuitry responsive to application of said DC voltage level disabling the second steering circuit.

4. A circuit in accordance with claim 1, further comprising:

circuitry responsive to application of a DC voltage level distorting the differential mode signal prior to transmitting it on the second pair of conductors.

5. A circuit in accordance with claim 1 wherein said first steering circuit comprises:

an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

6. A circuit in accordance with claim 5 wherein said second steering circuit comprises an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

7. A circuit in accordance with claim 6, further comprising:

circuitry responsive to application of a DC voltage level disabling the first steering circuit.

8. A circuit in accordance with claim 7, further comprising:

circuitry responsive to application of said DC voltage level disabling the second steering circuit.

9. A circuit in accordance with claim 6, further comprising:

circuitry responsive to application of a DC voltage level distorting the differential mode signal prior to transmitting it on the second pair of conductors.

10. A circuit is accordance with claim 1 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

11. A circuit in accordance with claim 10 wherein said second steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

12. A circuit in accordance with claim 11, further comprising:

circuitry responsive to application of a DC voltage level disabling the first steering circuit.

13. A circuit in accordance with claim 12, further comprising:

circuitry responsive to application of said DC voltage level disabling the second steering circuit.

14. A circuit in accordance with claim 11, further comprising:

circuitry responsive to application of a DC voltage level distorting the differential mode signal prior to transmitting it on the second pair of conductors.

15. A circuit in accordance with claim 1, further comprising:

a current mirror associated with said first steering circuit;

a voltage storage device coupled to said current mirror; and

a switch controlled by a voltage stored on said voltage storage device, said switch coupled to said second steering circuit for altering operation of said second steering circuit in response to the voltage stored on said voltage storage device.

16. A circuit in accordance with claim 1, further comprising:

a current mirror associated with said first steering circuit;

a voltage storage device coupled to said current mirror; and

a switch controlled by a voltage stored on said voltage storage device, said switch coupled to said first steering circuit for altering operations of said first steering circuit in response to the voltage stored on said voltage storage device.

17. A circuit in accordance with claim 15 wherein said first steering circuit comprises:

an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

18. A circuit in accordance with claim 16 wherein said first steering circuit comprises:

an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

19. A circuit in accordance with claim 17 wherein said second steering circuit comprises an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

20. A circuit in accordance with claim 18 wherein said second steering circuit comprises an NPN bipolar transistor and a PNP bipolar transistor having their respective emitters and collectors mutually coupled.

21. A circuit is accordance with claim 15 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

22. A circuit is accordance with claim 16 wherein said first steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

23. A circuit in accordance with claim 21 wherein said second steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

24. A circuit in accordance with claim 22 wherein said second steering circuit comprises:

a P-channel MOSFET and an N-channel MOSFET having their respective drains and sources mutually coupled.

25. A method for controlling the loop back of a differential mode signal received at a network device on a first pair of conductors and transmitted from the network device on a second pair of conductors, the method comprising:

receiving the differential mode signal;

applying the differential mode signal to a first steering circuit and a second steering circuit;

generating a first signal to be transmitted on a first one of the second pair of conductors with said first steering circuit; and

generating a second signal to be transmitted on a second one of the second pair of conductors with said second steering circuit.

26. A method in accordance with claim 25, further comprising:

transmitting said first and second signals on the second pair of conductors.

27. A method in accordance with claim 26, further comprising:

receiving at the network device a power signal; and

disabling at least one of said first steering circuit and said second steering circuit in response to receipt of said power signal.

28. A method in accordance with claim 26, further comprising:

receiving at the network device a power signal; and

distorting at least one of said first signal and said second signal in response to receipt of said power signal.

29. A method in accordance with claim 26, further comprising:

mirroring current from at least one of said first steering circuit and said second steering circuit;

rectifying said mirrored current;

applying said rectified current to a voltage storage device;

using said voltage storage device to control at least one switch; and

disabling at least one of said first steering circuit and said second steering circuit with said at least one switch.

30. A method in accordance with claim 26, further comprising:

mirroring current from at least one of said first steering circuit and said second steering circuit;

rectifying said mirrored current;

applying said rectified current to a voltage storage device;

using said voltage storage device to control at least one switch; and

distorting at least one of said first signal and said second signal with said at least one switch.

31. An apparatus for controlling the loop back of a differential mode signal received at a network device on a first pair of conductors and transmitted from the network device on a second pair of conductors, the apparatus comprising:

means for receiving the differential mode signal;

means for applying the differential mode signal to a first steering circuit and a second steering circuit;

means for generating a first signal to be transmitted on a first one of the second pair of conductors with said first steering circuit; and

means for generating a second signal to be transmitted on a second one of the second pair of conductors with said second steering circuit.

32. An apparatus in accordance with claim 31, further comprising:

means for transmitting said first and second signals on the second pair of conductors.

33. An apparatus in accordance with claim 32, further comprising:

means for receiving at the network device a power signal; and

means for disabling at least one of said first steering circuit and said second steering circuit in response to receipt of said power signal.

34. An apparatus in accordance with claim 32, further comprising:

means for receiving at the network device a power signal; and

means for distorting at least one of said first signal and said second signal in response to receipt of said power signal.

35. An apparatus in accordance with claim 32, further comprising:

means for mirroring current from at least one of said first steering circuit and said second steering circuit;

means for rectifying said mirrored current;

means for applying said rectified current to a voltage storage device;

means for using said voltage storage device to control at least one switch; and

means for disabling at least one of said first steering circuit and said second steering circuit with said at least one switch.

36. An apparatus in accordance with claim 32, further comprising:

means for mirroring current from at least one of said first steering circuit and said second steering circuit;

means for rectifying said mirrored current;

means for applying said rectified current to a voltage storage device;

means for using said voltage storage device to control at least one switch; and

means for distorting at least one of said first signal and said second signal with said at least one switch.